In the Specification:

Please amend Paragraph 30 as follows:

Core I/O pins 275 are electrically connected to backside chip I/O pads 280 by conductive backside vias 285 formed in substrate 205, device level 215 and M1 level 220. Each conductive backside via 285 includes an insulating liner 290, a conductive liner 295 and a bulk conductor 300. Insulating liner 290 insulates conductive backside via 285 from substrate 205. Backside chip I/O pads 280 and conductive backside vias 285 are included in the design of core 260 and form part the core. As shown in FIG. 3, the backside via 285 may have sloped sidewalls; i.e., the sidewalls of the backside via 285 in FIG. 3 are inclined and not perpendicular to the backside chip I/O pad 280. In addition, the backside chip I/O pad 280 is shown in FIG. 3 as being in direct mechanical contact with bulk conductor 300 that is comprised by the backside via 28. However, a portion of the backside chip I/O pad 280 is shown in FIG. 3 as not in direct mechanical contact with the backside via 28 and in direct mechanical contact with the backside surface of the integrated circuit chip 200.